AMENDMENTS TO CLAIMS:

The listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A lock detection circuit in communication with a phase lock loop to detect phase-frequency lock of an output frequency signal of said phase lock loop with an input reference signal, comprising:

a first logic function circuit to combine a frequency increase signal and a frequency decrease signal of said phase lock loop to provide a frequency deviation signal; ~~and~~

a second logic function circuit to combine the frequency deviation signal with the input reference signal to determine that the frequency deviation signal has a greater duration than a portion of a cycle of said input reference signal and provide an error signal; and

an integrator circuit in communication with the second logic function to receive and integrate the error signal and upon the error signal achieving an integrated threshold level, transferring an unlock alarm indicating loss of phase-frequency lock of said phase lock loop.

2. (Cancel)

3. (Cancel)

4. (Original) The lock detection circuit of claim 1 further comprising a frequency divider connected to receive the input reference signal, divide said input reference signal, and transfer the divided input reference signal to the second function circuit, wherein said second logic function circuit combines the deviation signal and the divided input reference signal to generate the error signal.

5. (Original) The lock detection circuit of claim 1 wherein the first logic function circuit is an OR gate.

6. (Original) The lock detection circuit of claim 1 wherein the second logic function circuit is an AND gate.

7. (Currently Amended) A lock detection circuit ~~in~~ for communication with a phase lock loop to detect phase-frequency lock of an output frequency signal of said phase lock loop with an input reference signal to said phase lock loop, wherein said phase lock loop includes a first phase-frequency detector, a charge pump responsive to said first phase-frequency detector, and a variable oscillator responsive to said charge pump, wherein said first phase-frequency detector is coupled to receive a first input proportional to said output frequency signal and a second input proportional to said reference signal to generate a first frequency increase signal and a first frequency decrease signal indicative of an amount of phase-frequency deviation of said first and second input signals, said lock detection circuit comprising:

a second phase-frequency detector ~~in communication with the phase lock loop~~ coupled to receive a third input proportional to said ~~the~~ output frequency signal and a fourth input proportional to ~~the~~ said ~~input~~ reference signal to generate a second frequency increase signal and a second frequency decrease signal indicative of an amount of phase-frequency deviation of said third and fourth inputs ~~the output frequency signal has from the input reference signal~~;

a first logic function circuit connected to the second phase frequency detector to combine said second ~~a~~ frequency increase signal and ~~a~~ said second frequency decrease signal to provide a frequency deviation signal; and

a second logic function circuit to combine the frequency deviation signal with a clocking signal proportional to the input reference signal to determine that the frequency deviation signal has a greater duration than a portion of a cycle of said ~~input reference signal~~ clocking signal and provide an error signal.

8. (Original) The lock detection circuit of claim 7 wherein the first logic function circuit is an OR gate.

9. (Original) The lock detection circuit of claim 7 wherein the second logic function circuit is an AND gate.

10. (Currently Amended) A phase lock loop system comprising:

a phase lock loop having a first phase-frequency detector and a variable oscillator responsive to said first phase-frequency detector for producing an output frequency signal, wherein said first phase-frequency detector is coupled to receive a first input proportional to said output frequency signal and a second input proportional to a reference signal to generate a first frequency increase signal and a first frequency decrease signal indicative of an amount of phase-frequency deviation of said first and second input signals

~~a phase-frequency detector to detect a difference in frequency between an output frequency of said phase lock loop and an input reference frequency of said phase lock loop~~; and

a lock detection circuit to detect loss of phase-frequency lock of the output frequency signal of said phase lock loop with the input reference signal and upon detection of said loss of phase-frequency lock provide an unlock alarm, said lock detection circuit comprising:

a second phase-frequency detector coupled to receive a third input proportional to said output frequency signal and a fourth input proportional to said reference signal to generate a second frequency increase signal and a second frequency decrease signal indicative of an amount of phase-frequency deviation of said third and fourth inputs;

a first logic function circuit to combine ~~a~~ said second frequency increase signal and ~~a~~ said second frequency decrease signal ~~received from said phase-frequency detector~~ to provide a frequency deviation signal; and

a second logic function circuit to combine the frequency deviation signal with a clocking signal proportional to the input reference signal to determine that the frequency deviation signal has a greater duration than a portion of a cycle of said ~~input reference signal~~ clocking signal and provide said unlock alarm.

11. (Currently Amended) The phase lock loop of claim 10 wherein the lock detection circuit further comprises a latching circuit in communication with the second logic function ~~and the input reference signal~~ to capture and retain said

unlock alarm to provide an unlock alarm signal indicating loss of phase-frequency lock of said phase lock loop.

12. (Currently Amended) ~~The phase lock loop of claim 10~~ A phase lock loop system comprising:

a phase-frequency detector to detect a difference in frequency between an output frequency of said phase lock loop and an input reference frequency of said phase lock loop; and

a lock detection circuit to detect loss of phase-frequency lock of the output frequency signal of said phase lock loop with the input reference signal and upon detection of said loss of phase-frequency lock provide an unlock alarm, said lock detection circuit comprising:

a first logic function circuit to combine a frequency increase signal and a frequency decrease signal received from said phase-frequency detector to provide a frequency deviation signal; and

a second logic function circuit to combine the frequency deviation signal with the input reference signal to determine that the frequency deviation signal has a greater duration than a portion of a cycle of said input reference signal and provide said unlock alarm;

wherein the lock detection circuit further comprises an integrator circuit in communication with the second logic function to receive and integrate the error signal and upon the error signal achieving an integrated threshold level, transferring an unlock alarm indicating loss of phase-frequency lock of said phase lock loop.

13. (Original) The phase lock loop of claim 10 wherein the lock detection circuit further comprises a frequency divider connected to receive the input reference signal, divide said input reference signal, and transfer the divided input reference signal to the second function circuit, wherein said second logic function circuit combines the deviation signal and the divided input reference signal to generate the error signal.

14. (Original) The phase lock loop of claim 10 wherein the first logic function circuit is an OR gate.

15. (Original) The phase lock loop of claim 10 wherein the second logic function circuit is an AND gate.

16. (Cancel)

17. (Cancel)

18. (Cancel)

19. (Currently Amended) A clock extraction circuit to provide an alarm indicating that a local oscillator signal is no longer in phase-frequency synchronism with an reference timing signal extracted from a data stream, said clock extraction circuit comprises:

a clock extractor to remove said timing signal from said data stream;

a phase lock loop in communication with the clock extractor to receive said timing signal and adjust a phase and frequency of the local oscillator signal synchronize said local oscillator signal to the timing signal; and

a lock detection circuit to detect loss of phase-frequency lock of the local oscillator signal with the timing signal and upon detection of said loss of phase-frequency lock provide an unlock alarm, said lock detection circuit comprising:

a first logic function circuit to combine a frequency increase signal and a frequency decrease signal received from said phase lock loop to provide a frequency deviation signal, and

a second logic function circuit to combine the frequency deviation signal with the timing signal to determine that the frequency deviation signal has a greater duration than a portion of a cycle of said timing signal and provide said unlock alarm;

wherein the lock detection circuit further comprises an integrator circuit in communication with the second logic function to receive and integrate the error signal and upon the error signal achieving an integrated threshold level, transferring an unlock alarm indicating loss of phase-frequency lock of said phase lock loop.

20. (Cancel)

21. (Cancel)

22. (Original) The clock extractor of claim 19 wherein the lock detection circuit further comprises a frequency divider connected to receive the input reference signal, divide said input reference signal, and transfer the divided input reference signal to the second function circuit, wherein said second logic function circuit combines the deviation signal and the divided input reference signal to generate the error signal.

23. (Original) The clock extractor of claim 19 wherein the first logic function circuit is an OR gate.

24. (Original) The clock extractor of claim 19 wherein the second logic function circuit is an AND gate.

25-36. (Cancel)

37. (Original) A synchronous communication system for the transfer of a synchronous transport signal, comprising:

synchronous transmission apparatus to combine a data signal and a timing reference signal to form the synchronous transport signal; and

synchronous communication receiver apparatus in communication with the synchronous transmission apparatus to receive the synchronous transport signal band to extract said data and the reference timing signal, comprising:

a receiver to receive and buffer said synchronous transport signal,

a clock extraction circuit in communication with the receiver to receive the synchronous transport signal and to provide an alarm indicating that a local oscillator signal is no longer in phase-frequency synchronism with the reference timing signal extracted from a synchronous transport signal, said clock extraction circuit comprises:

a clock extractor to remove said timing signal from said synchronous transport signal,

a phase lock loop in communication with the clock extractor to receive said reference timing signal and adjust a phase and frequency of the local oscillator signal synchronize said local oscillator signal to the timing signal, and

a lock detection circuit to detect loss of phase-frequency lock of the local oscillator signal with the timing signal and upon detection of said loss of phase-frequency lock provide an unlock alarm, said lock detection circuit comprising:

a first logic function circuit to combine a frequency increase signal and a frequency decrease signal received from said phase lock loop to provide a frequency deviation signal, and

a second logic function circuit to combine the frequency deviation signal with the timing signal to determine that the frequency deviation signal has a greater duration than a portion of a cycle of said timing signal and provide said unlock alarm.

38. (Original) The synchronous communication system of claim 37 wherein the lock detection circuit further comprises a latching circuit in communication with the second logic function and the input reference signal to capture and retain said unlock alarm to provide an unlock alarm signal indicating loss of phase-frequency lock of said phase lock loop.

39. (Original) The synchronous communication system of claim 37 wherein the lock detection circuit further comprises an integrator circuit in communication with the second logic function to receive and integrate the error signal and upon the error signal achieving an integrated threshold level, transferring an unlock alarm indicating loss of phase-frequency lock of said phase lock loop.

40. (Original) The synchronous communication system of claim 37 wherein the lock detection circuit further comprises a frequency divider connected to receive the input reference signal, divide said input reference signal, and transfer the divided input reference signal to the second function circuit, wherein said second logic function circuit combines the deviation signal and the divided input reference signal to generate the error signal.

41. (Original) The synchronous communication system of claim 37 wherein the first logic function circuit is an OR gate.

42. (Original) The synchronous communication system of claim 37 wherein the second logic function circuit is an AND gate.

43. (Original) The synchronous communication system of claim 37 wherein said synchronous communication system is a SONET communication system.

44. (Original) A synchronous communication system for the transfer of a synchronous transport signal, comprising:

a synchronous transmission apparatus to combine a data signal and a timing reference signal to form the synchronous transport signal;

a synchronous communication receiver apparatus in communication with the synchronous transmission apparatus to receive the synchronous transport signal band to extract said data and the reference timing signal, comprising:

a receiver to receive and buffer said synchronous transport signal,

a clock extraction circuit in communication with the receiver to receive the synchronous transport signal and to provide an alarm indicating that a local oscillator signal is no longer in phase-frequency synchronism with the reference timing signal extracted from a synchronous transport signal, said clock extraction circuit comprises:

a clock extractor to remove said timing signal from said synchronous transport signal,

a phase lock loop in communication with the clock extractor to receive said reference timing signal and adjust a phase and frequency of the local oscillator signal synchronize said local oscillator signal to the timing signal; and

a lock detection circuit to detect loss of phase-frequency lock of the local oscillator signal with the timing signal and upon detection of said loss of phase-frequency lock provide an unlock alarm, said lock detection circuit comprising:

a phase-frequency detector in communication with the phase lock loop to receive the output frequency signal and the input reference signal to generate a frequency increase signal and a frequency decrease signal indicative of an amount of phase-frequency deviation of the output frequency signal has from the input reference signal,

a first logic function circuit connected to the phase frequency detector to combine a frequency increase signal and a frequency decrease signal to provide a frequency deviation signal, and

a second logic function circuit to combine the frequency deviation signal with the timing signal to determine that the frequency deviation signal has a greater duration than a portion of a cycle of said timing signal and provide said unlock alarm.

45. (Original) The synchronous communication system of claim 44 wherein the first logic function circuit is an OR gate.

46. (Original) The synchronous communication system of claim 44 wherein the second logic function circuit is an AND gate.

47. (Original) The synchronous communication system of claim 44 wherein said synchronous communication system is a SONET communication system.

48-56. (Cancel)

57. (New) The lock detection circuit of claim 7 further having a frequency divider with a frequency-dividing input coupled to receive said first input to said first phase-frequency detector, and having a frequency-dividing output coupled to said third input of said second phase-frequency detector.

58. (New) The lock detection circuit of claim 7 further having a frequency divider with a frequency-dividing input coupled to receive said second input to said first phase-frequency detector, and having a frequency-dividing output coupled to said fourth input of said second phase-frequency detector.

59. (New) The lock detection circuit of claim 10 further having a frequency divider with a frequency-dividing input coupled to receive said first input to said first phase-frequency detector, and having a frequency-dividing output coupled to said third input of said second phase-frequency detector.

60. (New) The lock detection circuit of claim 10 further having a frequency divider with a frequency-dividing input coupled to receive said second input to said first phase-frequency detector, and having a frequency-dividing output coupled to said fourth input of said second phase-frequency detector.